IN THE CLAIMS:

1. (Original) A method for manufacturing a trench isolation structure, comprising:

forming a polysilicon hardmask over a substrate;

etching a trench in said substrate through said polysilicon hardmask; and

filling said trench with an insulative material.

2. (Original) The method as recited in Claim 1 further including placing a pad oxide layer between said substrate and said polysilicon hardmask.

3. (Original) The method as recited in Claim 2 wherein said pad oxide layer has a thickness ranging from about 10 nm to about 20 nm.

4. (Original) The method as recited in Claim 1 further including growing a liner oxide within said trench and over said polysilicon hardmask prior to filling said trench with said insulative material.

5. (Original) The method as recited in Claim 4 wherein said grown liner oxide has a thickness ranging from about 10 nm to about 20 nm.

6. (Original) The method as recited in Claim 1 wherein filling said trench with an insulative material includes depositing said insulative material within said trench.

7. (Original) The method as recited in Claim 1 wherein said polysilicon hardmask has a thickness ranging from about 100 nm to about 200 nm.

8. (Original) The method as recited in Claim 1 wherein said trench has a width ranging from about .15 μm to about 20 μm and has a depth ranging from about 0.1 μm to about 0.5 μm.

9. (Original) A trench isolation structure formed using said method of Claim 1.

10. (Original) A method for manufacturing an integrated circuit, comprising:

forming trench isolation structures in a substrate, including;

forming a polysilicon hardmask over said substrate;

etching a trench in said substrate through said polysilicon hardmask; and

filling said trench with an insulative material;

forming transistor devices over said substrate; and

constructing an interlevel dielectric layer over said transistor devices and having interconnects located therein, wherein said interconnects contact said transistor devices to form an operational integrated circuit.

11. (Original) The method as recited in Claim 10 further including placing a pad oxide layer between said substrate and said polysilicon hardmask.

12. (Original) The method as recited in Claim 11 wherein said pad oxide layer has a thickness ranging from about 10 nm to about 20 nm.

13. (Original) The method as recited in Claim 10 further including growing a liner oxide within said trench and over said polysilicon hardmask prior to filling said trench with said insulative material.

14. (Original) The method as recited in Claim 13 wherein said grown liner oxide has a thickness ranging from about 10 nm to about 20 nm.

15. (Original) The method as recited in Claim 10 wherein filling said trench with an insulative material includes depositing said insulative material within said trench.

16. (Original) The method as recited in Claim 10 wherein said polysilicon hardmask has a thickness ranging from about 100 nm to about 200 nm.

17. (Original) The method as recited in Claim 10 wherein said trench has a width ranging from about .15 μm to about 20 μm and has a depth ranging from about 0.1 μm to about 0.5 μm.

18. (Original) An integrated circuit formed using said method of Claim 10.

Claims 19-20 (Canceled)

Respectfully submitted,

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